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(71) Applicant: **SEIKO EPSON CORP**

(72) Inventor: **OKA HIDEAKI**

(74) Representative:

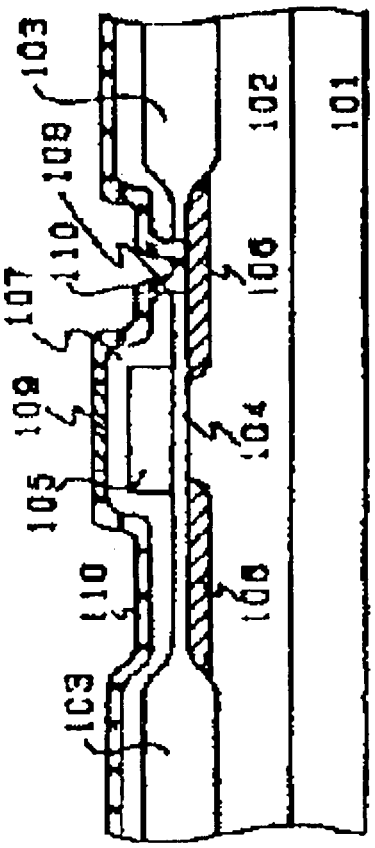
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57) Abstract:

PURPOSE: To reduce the OFF current of an insulated gate type field effect transistor by a method wherein a fluorine content in a polycrystalline semiconductor layer is controlled to be not higher than 1×1018/cm3.

CONSTITUTION: A polycrystalline semiconductor layer 109 mainly

made of silicon is formed on an insulating layer 107 which is to be a gate insulating film. The polycrystalline semiconductor layer 109 is formed by a plasma CVD method with mixed gas composed of monosilane, disilane, trisilane or the like and hydrogen gas with a ratio of 1:20-1:200 as reactive gas. Then fluorine ions are implanted as impurities to form source/drain regions 110. The source/drain regions 110 formed by ion implantation are activated by annealing. A fluorine content in the polycrystalline semiconductor layer 109 is so controlled as to be not higher than 1×1018/cm3. It is to be noted that the annealing treatment for the activation is performed in a plurality of times with different temperatures respectively. With this constitution, the OFF current of an insulated gate type field effect transistor can be reduced.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